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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,763	01/31/2006	Godefridus Johannes Gertrudis Maria Geelen	NL 030935	6167

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CHENG, DIANA	
ART UNIT	**PAPER NUMBER**
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,763	GEELEN, GODEFRIDUS JOHANNES GERTRUDIS M	
	Examiner	Art Unit	
	Diana J. Cheng	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "an input" in line 1, and further recites the limitation "an input signal" in line 3, where it is unclear whether both "input" are the same or different. Furthermore, it is unclear which input "said input signal" in lines 3-4 is in reference to. There is insufficient antecedent basis for this limitation in the claim.

For the purposes of this examination, "an input" in line 1 and "an input signal" in lines 3-4 will be interpreted as "an input" (line 1) and "a second input signal" (line 3), where the "said input signal" (lines 3-4) will be in reference to the second input signal.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Dedic (5,384,570).

Re claim 1, Dedic discloses a track-and-hold circuit in Fig. 3 having an input (Vin) [Vi] and an output signal (Vs) [Vo], a bootstrap switch (14a) [4] having as its inputs a clock signal [CK] and a second input signal (Vin) [Vhigh], said input signal (Vin) [Vhigh] being connected to said output signal (Vs) [Vo] of said circuit via level shifting (20) [Fig. 2, 33; Fig. 4, cascoded source follower 31] and buffering means (30) [Fig. 2, 32; Fig. 4, a current source 32], characterized in that said input signal of said bootstrap switch (14a) [4, 5] comprises said output signal (Vs) [Vo] of said circuit [Vo is connected to 4].

Re claim 2, Dedic discloses a track-and-hold circuit according to claim 1, including two or more bootstrap switches (14a, 14b) [Fig. 11, 4,5 included in VSC1,

VSC2], the input signal of each of which is connected to said output signal (Vs) [Vo] of said circuit via said level shifting (20) [Fig. 7, where in 31, L1 and L2 are connected to 4,5] and buffering means (30) [32].

Re claim 3, Dedic discloses a track-and-hold circuit according to claim 1, wherein said buffering means (30) comprises a MOS transistor [Fig. 2, 33; Fig. 4, 31].

Re claim 4, Dedic discloses a track-and-hold circuit according to claim 3, wherein said MOS transistor (30) is a PMOS transistor [Fig. 4, 33, 34].

Re claim 5, Dedic discloses a track-and-hold circuit in Fig. 3 according to claim 1, further comprising a capacitor (12) [2], said input signal being connected to said capacitor (12) via a switch (10) [Vi through 1 to 2], said switch (10) [1] being closed during a track mode of said circuit and open during a hold mode of said circuit [Col. 1, lines 14-30].

Re claim 8, Dedic discloses an analog-to-digital converter including a track-and-hold circuit according to claim 1 [Col. 1, lines 6-9].

Re claim 9, Dedic discloses an integrated circuit including an analog-to-digital converter according to claim 8 [where it would be inherent for an analog-to-digital converter be used in an integrated circuit].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570) as applied to claim 5 above, and further in view of Jensen et al. (US 2002/0084808 A1)

Re claim 6, Dedic teaches a track-and-hold circuit according to claim 5, but does not teach the rest of the claim.

Jensen et al. teaches a track and hold circuit in Fig. 2 further comprising one or more dummy switches (16) [56 and 58] which are clocked in anti-phase [A#] to said switch (10) [52, 54] connecting said input signal (Vin) [INPUT] to said capacitor (12) [46].

Dedic and Jenson et al. both teach a track and hold circuit. Jenson further teaches the use of cancellation transistors, which are equivalent to dummy transistors. In [0008], Jenson et al. teaches "one or more 'cancellation' transistors are employed within the switch circuit to dump charge of an opposite polarity (e.g., negative charge rather than positive charge) onto the circuit node at approximately the same time to reduce or eliminate the effects of the charge dumped by the switching transistors." Therefore, it would be obvious to improve the track and hold circuit of Dedic to further include the cancellation transistors as taught by Jenson et al, in order to eliminate the effects of the charge dumped by the switching transistors.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570) and Jensen et al. (US 2002/0084808 A1), as a whole, as applied to claim 6 above, and further in view of Fig. 3 as depicted in applicant admitted prior art (AAPA).

Re claim 7, Dedic and Jenson et al., as a whole, teach a track-and-hold circuit according to claim 6, but does not teach the rest of the claim.

The AAPA teaches in Fig. 3 the track and hold circuit wherein said input signal (Vin) is connected to said dummy switches (16) via a bootstrap switch (14b), having as an additional input an anti-phase clock signal.

Dedic and Jenson et al., as a whole, teach A# input into the dummy switches but do not where it is inputted from. The AAPA does. Therefore, it would be obvious to one of ordinary skill in the art to use a second bootstrap circuit of the AAPA to supply the A#

input, as taught in Dedic and Jenson et al, as a whole.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J. Cheng whose telephone number is (571) 270-1197. The examiner can normally be reached on Monday-Friday, 7:30am-5:00 pm, alt. Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Diana J Cheng
Examiner
Art Unit 2816

LINH MY NGUYEN
PRIMARY EXAMINER